REMARKS

Claims 1-24 are pending. Claims 1 - 8 have been amended herein and no new matter has been introduced. Claims 9 – 24 have been cancelled herein. New Claims 25 –36 have been added. No new matter has been added to the Specification.

Response to Restriction Requirement

In the Office Action mailed May 16, 2003, the Examiner states that the present Application contains four distinct inventions related as a process and apparatus for its practice. As such, the Examiner is requiring the Applicants to elect a single invention for examination. Specifically, the Examiner is requiring the Applicants to elect between a first invention, Group I, recited in Claims 1- 8, drawn to a method for testing wire bonds, classified in class 438, subclass 17; a second invention Group II. recited in Claims 9 – 13 and drawn to an integrated circuit packaging device with substrate, classified in class 438, subclass 106; a third invention, Group III, recited in Claims 14 - 19, drawn to an array molded laminate substrate, classified in class 438, subclass 125; and a fourth invention, Group IV, recited in Claims 20- 24 and drawn to an array substrate, classified in class 438, subclass 107.

Applicants elect without traverse Group I, recited in Claims 1-8, drawn to a method of making a semiconductor device, classified in Class 438, subclass 17.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Claim Rejections

35 U.S.C. §102

Claims 1 and 4-8 have been rejected under 35 U.S.C. §102(b) as being anticipated by US patent 4,812,742 to Abel et al. Applicants have reviewed Examiner's arguments and the cited reference and respectfully traverse in the following fashion.

Regarding Claim 1, Examiner states that Abel et al. disclose a method for testing wire bonds in an integrated circuit package comprising bonding an integrated circuit silicon die to a

package substrate, forming a wire connection between a circuit contact pad in the integrated circuit silicon die and a lead contact pad in the package substrate, and testing the wire connection for detection of '"non-stick failure"' with a testing device, wherein the silicon substrate of the integrated circuit provides electrical continuity for the non-stick detection between the circuit contact pad and a dedicated contact pad in the package substrate which is electrically coupled to the testing device (Col. 2, lines 5- 29).

However, Claim 1 of the present invention claims "testing said wire connection for detection of non-stick failure with a testing device, wherein said silicon substrate of said integrated circuit provides electrical continuity" for the testing. Abel et al require a "test region in the package body which is spaced apart from the array of I/O pins" (Col. 2, lines 15-16) and "an array of test pins which is attached to the test region" (Col. 2, line 18-19) for the continuity required for testing.. The claimed embodiment of the present invention does not require a separate "test region" nor does it require an array of test pins because it enables and claims the use of the existing silicon substrate for the requisite continuity. Claim 1, therefore, distinguishes over the cited art reference as well as the dependent Claims depending from Claim 1.

Regarding Claim 5, the rejection states that Abel et al disclose a method comprising all the elements described above, wherein bonding the integrated circuit silicon die provides electrical continuity between the integrated circuit silicon die and the dedicated pads in the package substrate (Col. 2, lines 15- 25). However, the cited reference does not teach "bonding said integrated circuit silicon die and the dedicated pads," as claimed in the present invention. Rather, the cited reference discloses bonding an integrated circuit to "several layers thin flat layers of ceramic or epoxy-glass...laminated together to make ...the package body and the test portion" (Col. 2, lines 63-66) The present invention, as claimed in independent Claim 1 from which Claim 5 depends, claims the use of the silicon substrate as a conductive medium, obviating the need for the separate "test portion" taught in the cited reference. Claim 5, therefore also distinguishes over the cited art reference which teaches away from the embodiment claimed in Claim 5.

Regarding Claims 4 and 6 – 8, they depend from and further limit Claim 1 and therefore overcome the cited reference.

However, Claims 4 - 6 are amended in order to more particularly point out and distinctly claim the present invention. No new matter is added as a result of the amendments. Examiner's rejection of Claims 1 and 4 – 8 is, therefore, respectfully traversed.

35 U.S.C. §103

Claims 2 and 3 are rejected under 35 U.S.C. 1 03(a) as being unpatentable over Abel et al. in view of Brooks et al. (US-6,326,244 ). Examiner's rejections are traversed in the following fashion.

In regards to Claims 2 and 3, Abel et al. disclose a method of testing, but fail to teach how the integrated circuit die is bonded to the package substrate. Brooks et al. teach using electrically non-conductive, thermally conductive epoxy to bond the integrated circuit die to the package substrate (Col. 7, lines 21 - 35). The rejection avers that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method disclosed by Abel et al. by using an electrically nonconductive, thermally conductive epoxy to bond the integrated circuit die to the package substrate, as taught by Brooks et al., for the purpose of protecting the package components.

However, for the reasons stated above, Brooks et al and Abel et al fail to disclose the testing method claimed in the present claimed invention. Claim 2 of the present invention claims the use of "conductive epoxy" for bonding in order to achieve continuity for the testing claimed in Claim 1. Brooks et al, therefore, by teaching "electrically non-conductive" epoxy, teach away from the present invention's claimed conductive epoxy of Claim 2. Abel et al do not cure this defect. Furthermore, because the bonding techniques claimed in Claims 2 and 3 are further limitations to novel and non-obvious Claim 1, the combination of Abel and Brooks does not teach or suggest the claimed combination. Examiner's rejection of Claims 2 and 3 under 35 U.S.C. §103 is therefore overcome and allowance of the Claims is respectfully requested.

Conclusion

Claims 1-24 are pending in the instant application. Claims 4 - 6 have been amended herein and, as amended, are fully supported in the detailed description. Claims 9 – 24 have been cancelled herein. Claims 25 – 36 have been added. No new matter has been added to the specification.

Examiner's rejection of Claims 1 – 8 have been respectfully traversed and, in light of the above remarks, reconsideration of the rejected Claims is respectfully requested.

Applicants have reviewed the references which were cited but not relied upon. Applicants assert that these references fail to teach or suggest the present claimed invention.

Based on the arguments presented above, it is respectfully asserted that Claims 1 - 8 overcome the rejections of record and, therefore, allowance of these Claims is respectfully solicited.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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